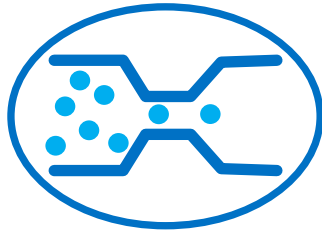


# TERATEC 2016

Isabelle Flory, WEUR Infrastructure Transformation Director  
June 2016

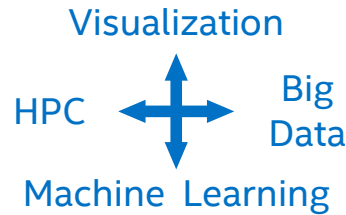
# Growing Challenges in System Architecture

## “The Walls” System Bottlenecks



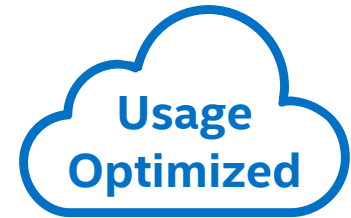
Memory | I/O | Storage  
Energy-Efficient Performance  
Space | Resiliency |  
Unoptimized Software

## Divergent Infrastructure



Resources Split Among  
Modeling and Simulation | Big  
Data Analytics | Machine  
Learning | Visualization

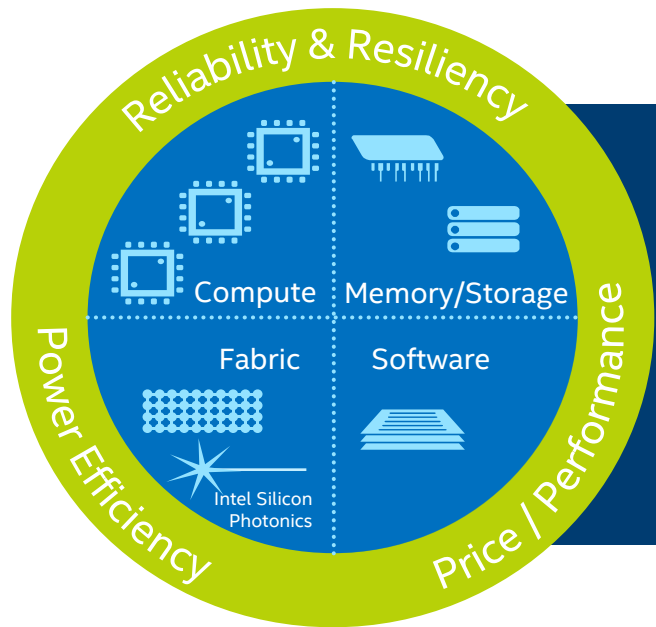
## Barriers to Extending Usage



Democratization at Every Scale |  
Cloud Access | Exploration of  
New Parallel Programming  
Models

# Fuel Your Insight

## Intel® Scalable System Framework



Small Clusters Through Supercomputers

Compute and Data-Centric Computing

Standards-Based Programmability

On-Premise and Cloud-Based

Intel® Xeon® Processors  
Intel® Xeon Phi™ Processors  
Intel® Xeon Phi™ Coprocessors  
Intel® Server Boards and Platforms

Intel® Solutions for Lustre\*  
Intel® Optane™ Technology  
3D XPoint™ Technology  
Intel® SSDs

Intel® Omni-Path Architecture  
Intel® True Scale Fabric  
Intel® Ethernet  
Intel® Silicon Photonics

Intel® HPC Orchestrator  
Intel® Software Tools  
Intel® Cluster Ready Program  
Intel Supported SDVis

# Intel® Xeon Phi™ Processor: Your Path to Deeper Insight

A Foundational Element of Intel® Scalable System Framework



Solve Biggest Challenges Faster

Highly-Parallel  
Eliminate Bottlenecks  
Scalability



Realize Compelling Value

Power Efficiency  
Programmability  
High Utilization



Maximize Future Potential

Future-Ready Code  
Broad Ecosystem  
Robust Roadmap

For discovery and business innovation in [science, visualization & analytics](#)

