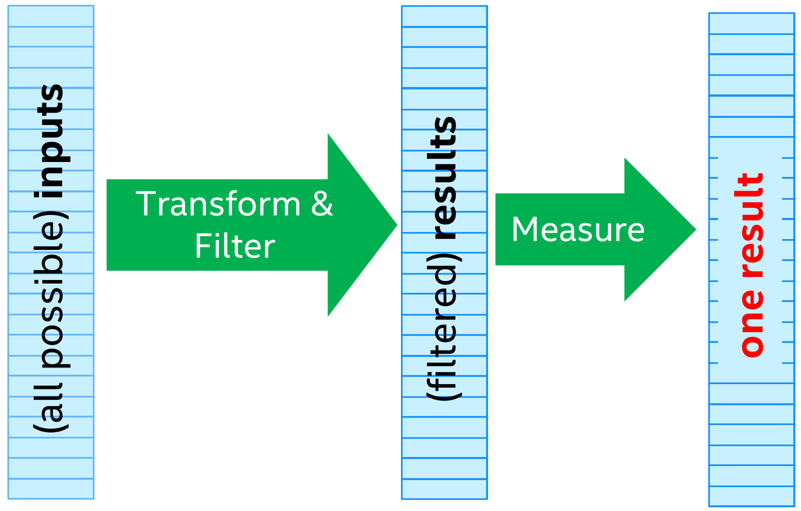
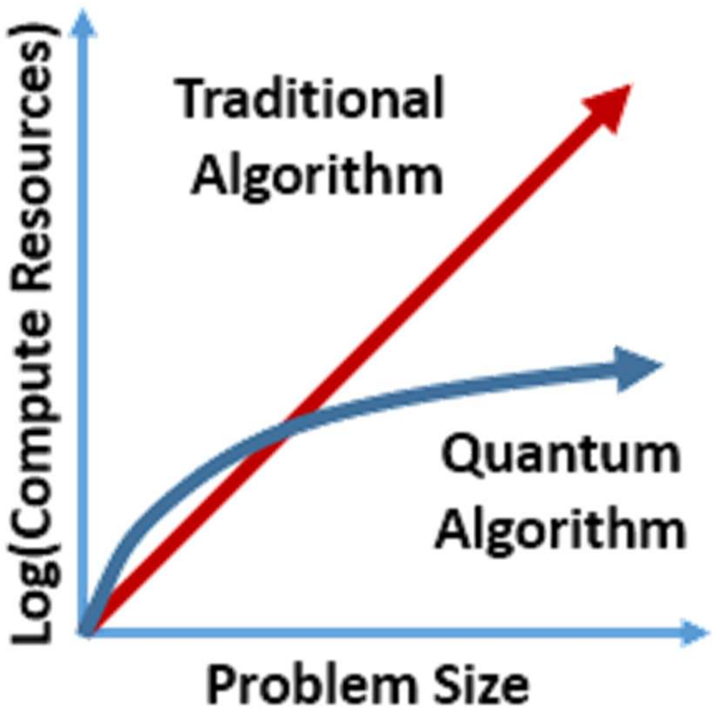
LEADING THE EVOLUTION OF COMPUTE: QUANTUM COMPUTING

Anne Matsuura, Ph.D.
Director, Quantum Applications & Architecture
Intel Labs

Teratec HPC Forum June 20, 2018

The promise of quantum computing





Exponential speedup ←→ surpassing the limits of scaling

Developing a Quantum Computer System

- **Application Algorithms**
- **Compilers/Runtimes**
- **Control Electronics**
- **Quantum Chip**

Challenges to be addresses at each level

Developing a Quantum Computer System

Application Algorithms

- Compelling Applications
- Resilient Algorithms
- Real Workloads for Early Systems

Compilers/Runtimes

Control Electronics

Quantum Chip

Applications Space: HPC

Quantum co-processor: augmenting, not replacing, traditional HPC systems

~50+ Qubits: Proof of concept

- Computational power exceeds supercomputers
- Learning test bed for quantum "system"

~1000+ Qubits: Small problems

- Limited error correction
- Chemistry, materials design
- Optimization

~1M+ Qubits: Commercial scale

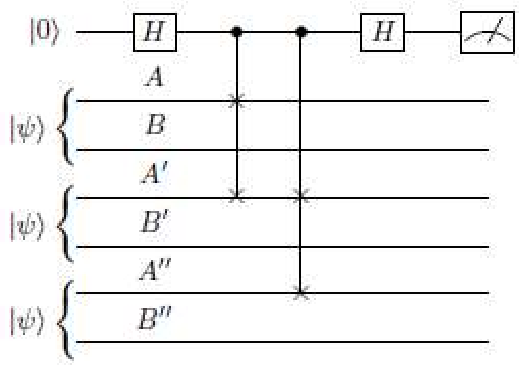
- Fault tolerant operation
- Cryptography
- Machine Learning

Materials Science

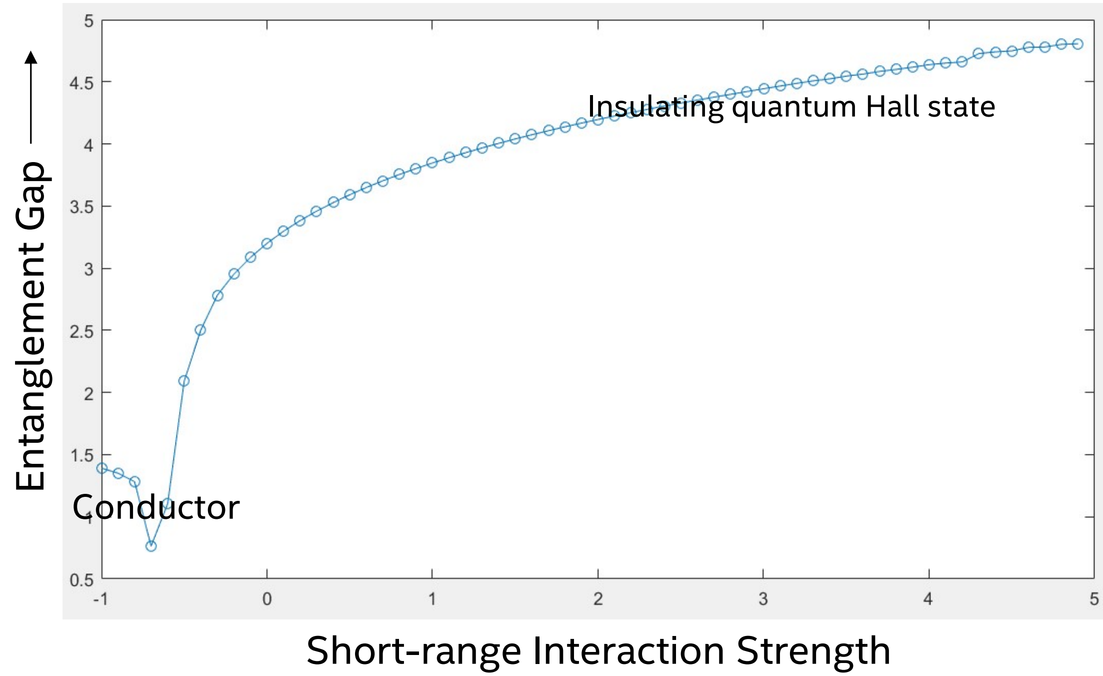
Quantifying entanglement provides a measurement of correlations between electrons which is useful for understanding the electronic properties of the material.

Algorithm to measure entanglement:

$$R_n = \langle\Psi|^{\otimes n} Per_A |\Psi\rangle^{\otimes n}$$



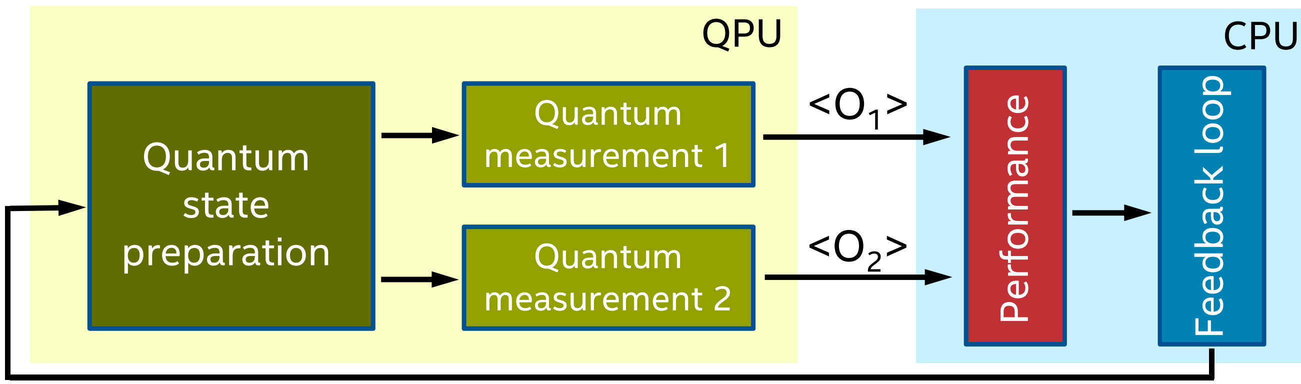
For example, in determining whether simulated material is a metal or an insulator.



Collaboration: *Damian Steiger, Matthias Troyer (ETH Zurich), Chris Monroe (U of MD)*

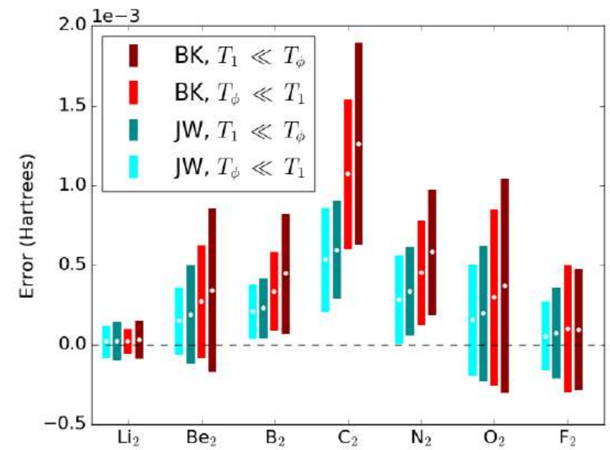
Resilient Algorithms

Hybrid quantum-classical



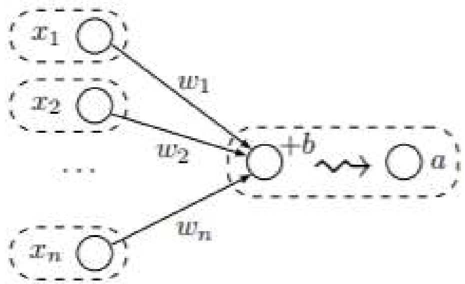
Quantum Chemistry and Noise study:

- Comparing two variants of the VQE algorithm to approximate lowest energy of molecules
- Surprisingly, version requiring more quantum operations is more resilient to noise

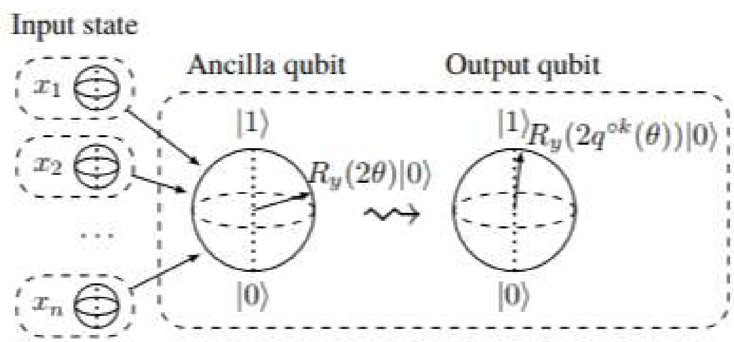


Collaboration: *Alan Aspuru-Guzik, Harvard, Jarrod McClean, LBL*

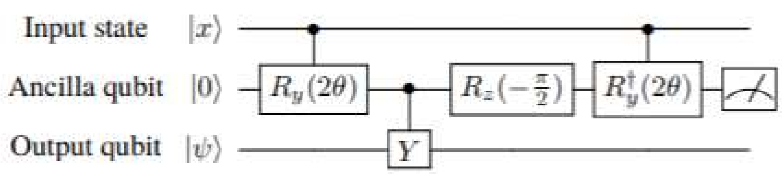
Machine Learning



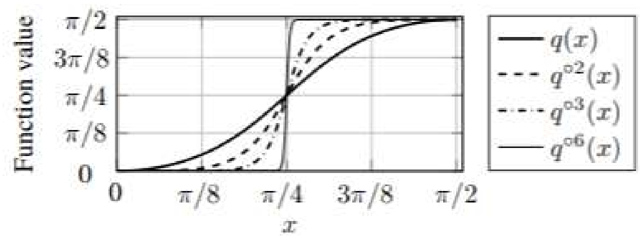
Classical Neuron



Quantum Neuron



Repeat Until Success
circuit



Non-linear Transfer
Function

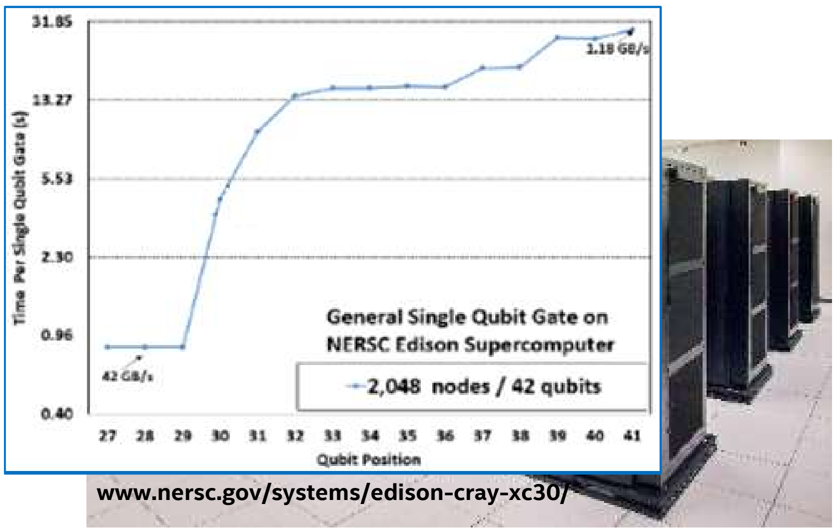
Collaboration: Yudong Cao and Alán Aspuru-Guzik, Harvard University

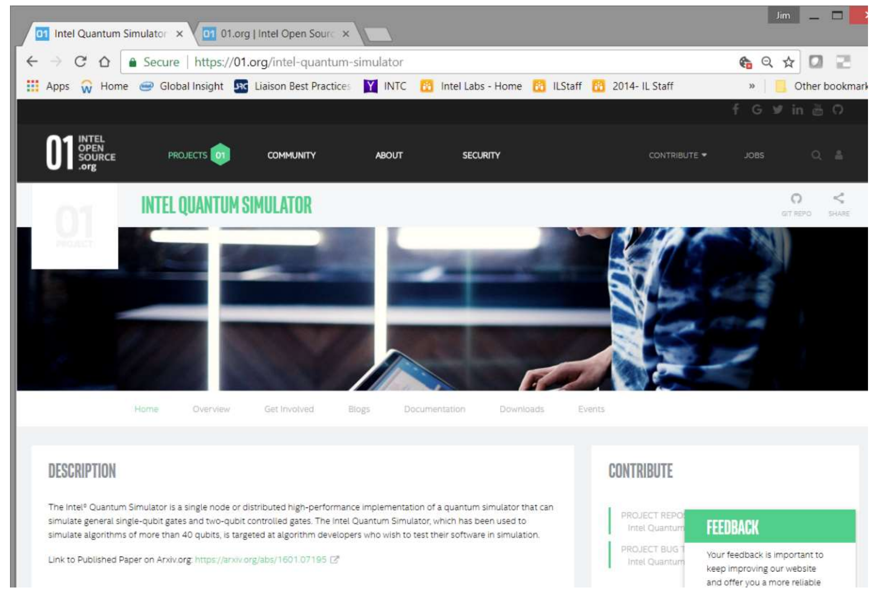
Qubit Simulation – Intel Quantum Simulator

Universal: single and two-qubit controlled gates

Open Source Release

High Perf QuBit Simulation





External Collaboration: *Alan Aspuru-Guzik (Harvard), Matthias Troyer (ETH Zürich)*

Developing a Quantum Computer System

- Application Algorithms
- Compilers/Runtimes
- Control Electronics
- Quantum Chip

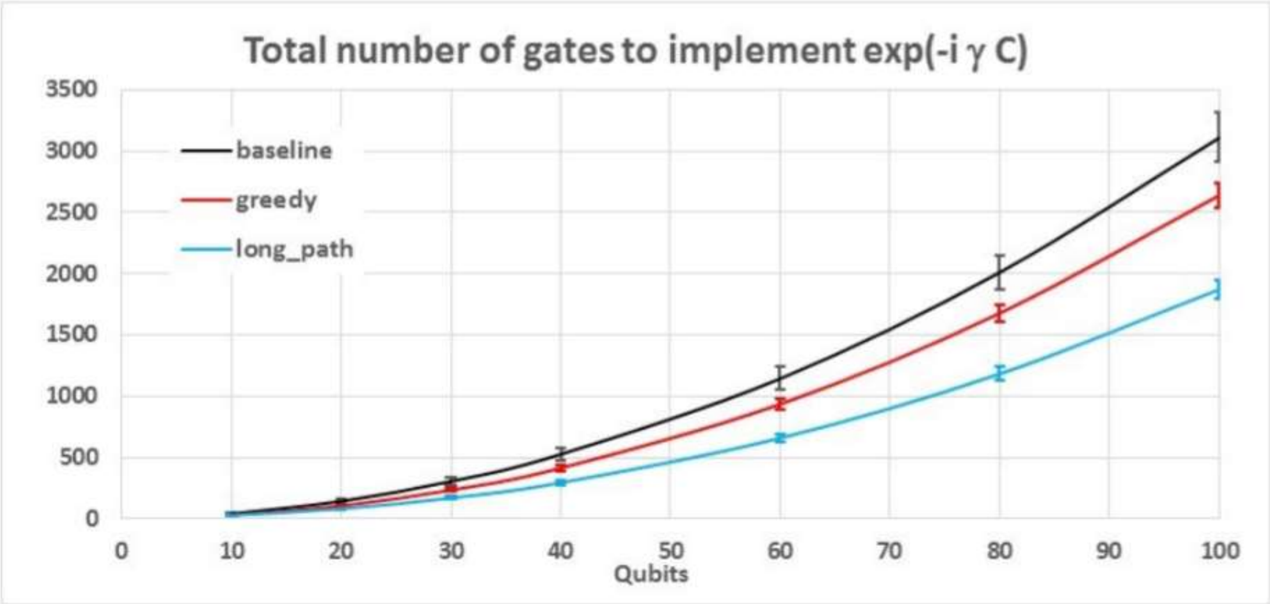
Compilers/Runtimes:

- Optimization
- Mapping & Scheduling
- Fault tolerant operations

Gate scheduling for quantum algorithms

Mapping and scheduling under constraints:

- Logical dependency
- Exclusive activation
- Physical connectivity



Scheduling Quantum Approximate Optimization Algorithm for hardware with linear connectivity: three strategies of increasing sophistication

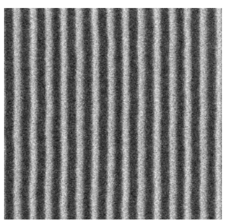
Intel – QuTech Research Collaboration

Intel Labs:

- Algorithms
- System Architecture
- Control Electronics

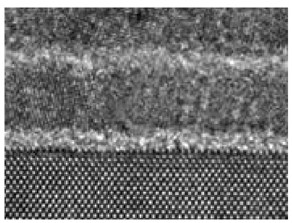
TMG Components Research

Patterning



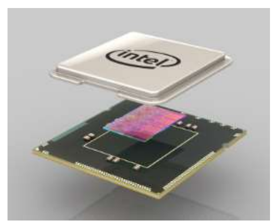
24nm Pitch Lines

Atomic Layer Control



Metal Gate / High k on 300mm Silicon Wafer

Packaging



Assembly and Packaging Research

QuTech's Expertise in qubit operation and control

Combining Intel capabilities with Delft expertise

Developing a Quantum Computer System

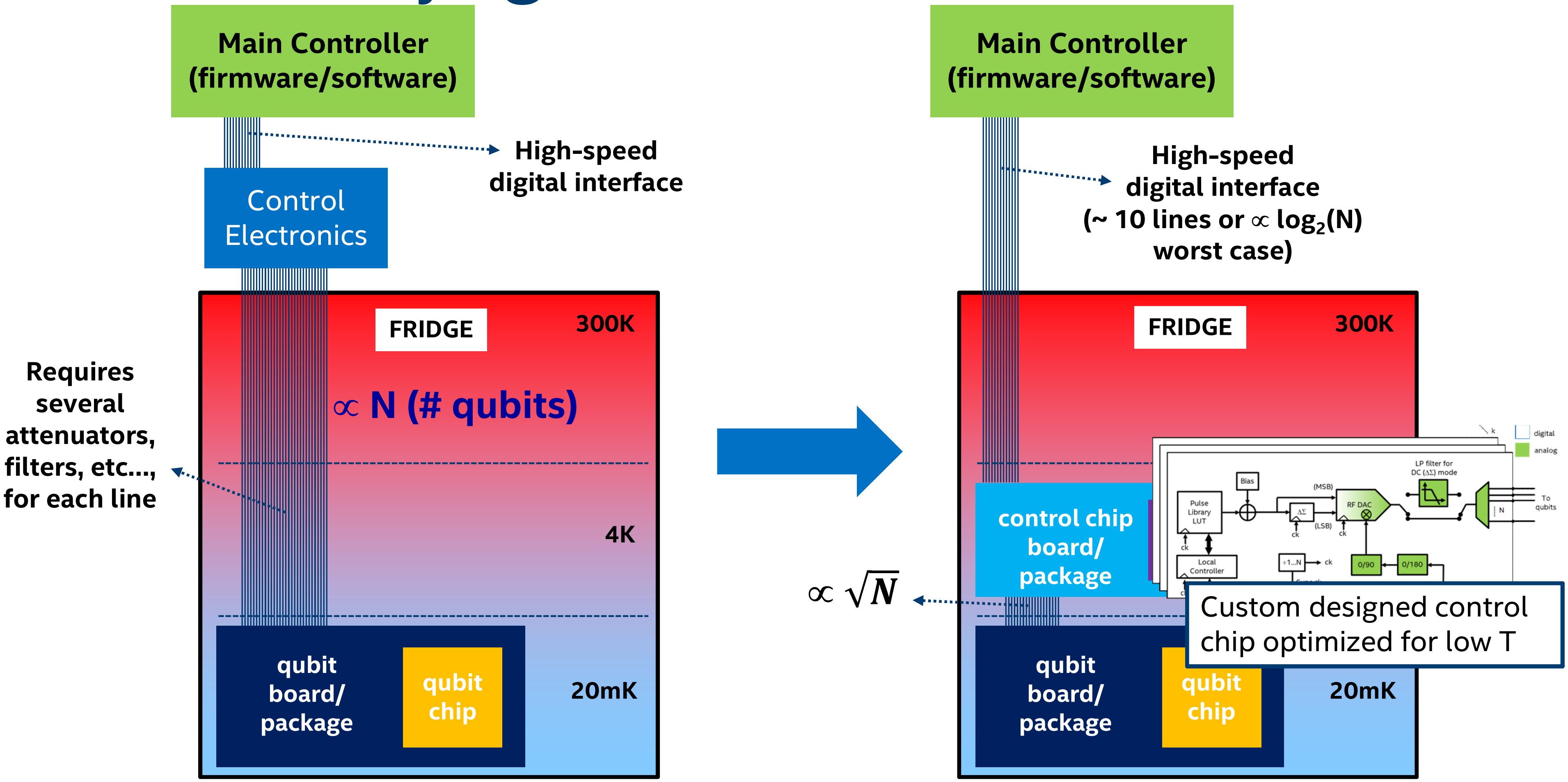
Application Algorithms

Compilers/Runtimes

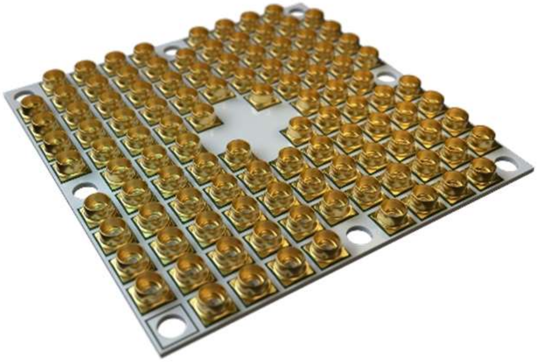
Control Electronics
- Digital/Analog Control
- Error Correction
- I/O to Qubit plane

Quantum Chip

Solution Cryogenic Control



Scaling I/O to the Qubit Plane



Processor
- 10^9 transistors
- 10^3 pins

3D NAND Memory
- 10^{12} bytes
- 10^2 pins

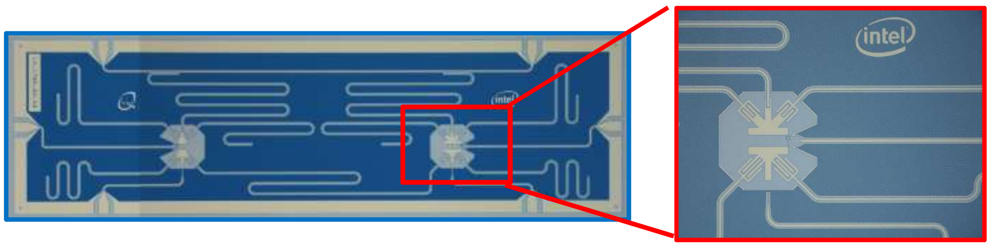
49-Qubit Transmon Array
- 49 qubits
- 108 pins

Developing a Quantum Computer System

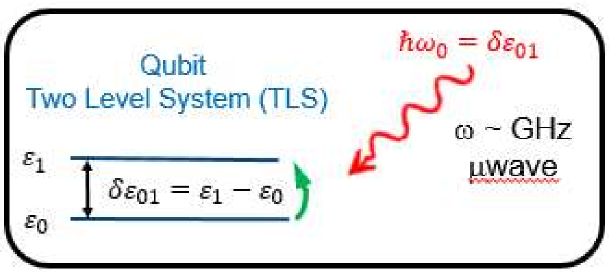
- **Application Algorithms**
- **Compilers/Runtimes**
- **Control Electronics**
- **Quantum Chip**
  - Qubit Device Design & Fabrication
  - Assembly & Packaging
  - Topology & Connectivity

Building Better Qubits

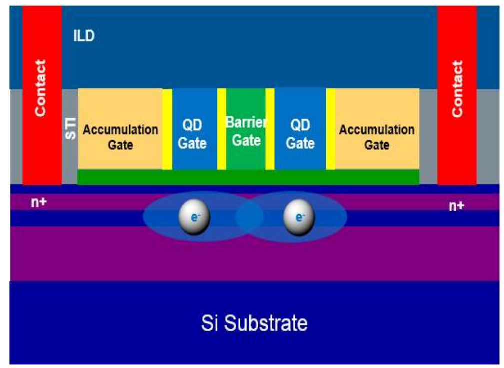
Superconducting Qubits

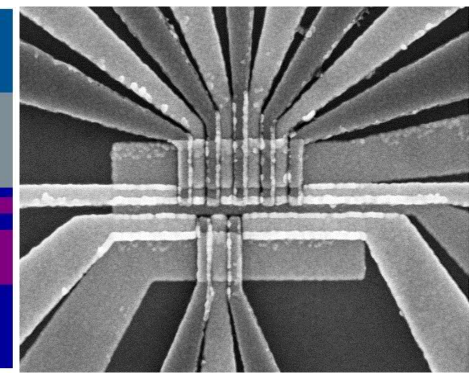


Very high quality microwave circuit

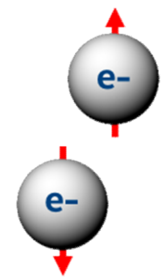


Spin Qubits in Silicon

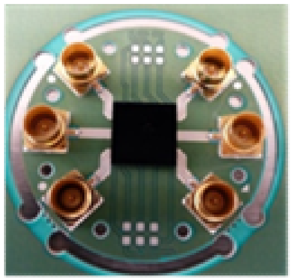




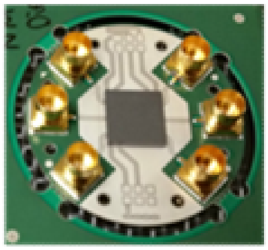
Single electron transistors, where qubit is spin state



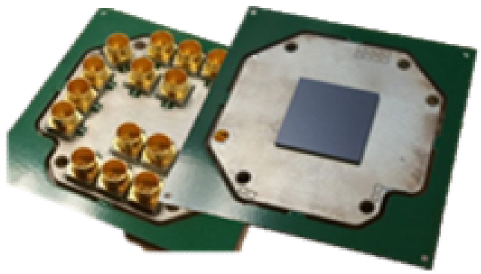
Superconducting Qubit Progress



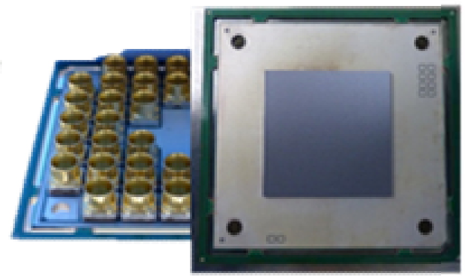
Resonator



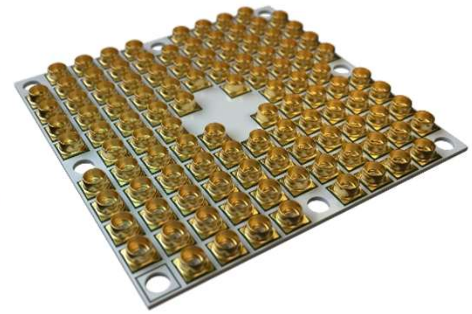
6 Qubits



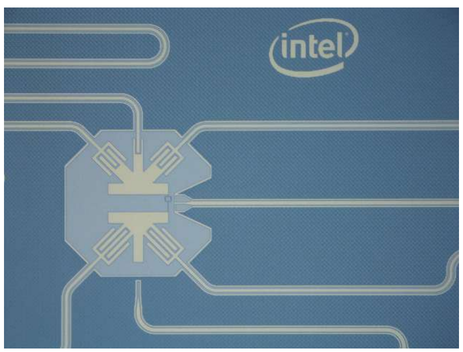
7 Qubit Array



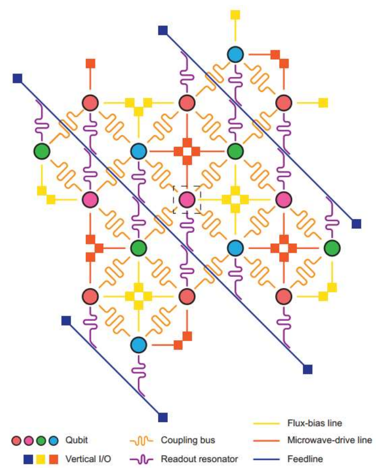
17 Qubit Array



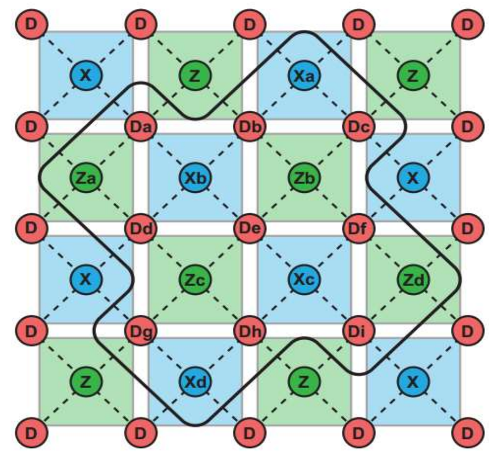
Tangle Lake



Starmon Geometry
with up to 30us T1

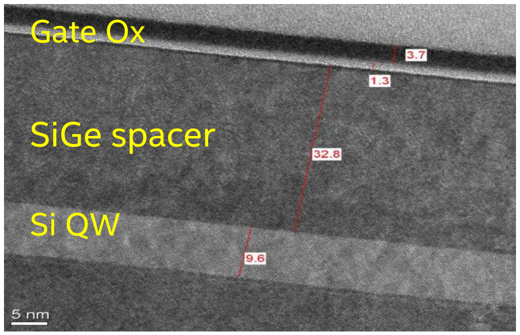


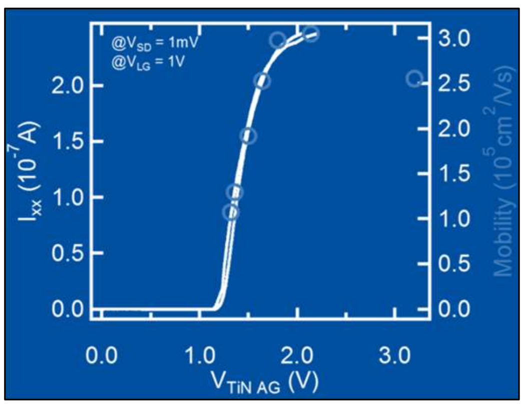
Shared Feedlines



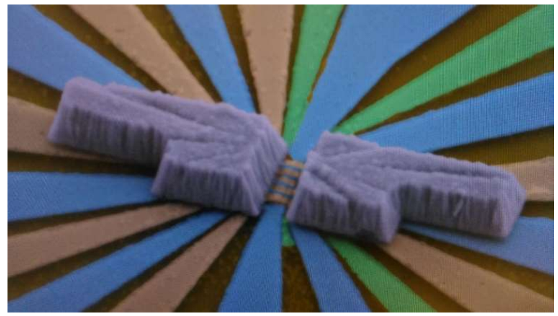
Surface Code Topology

Spin Qubits In Silicon

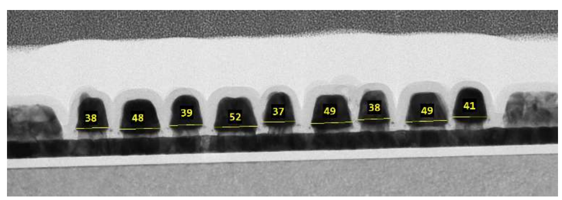


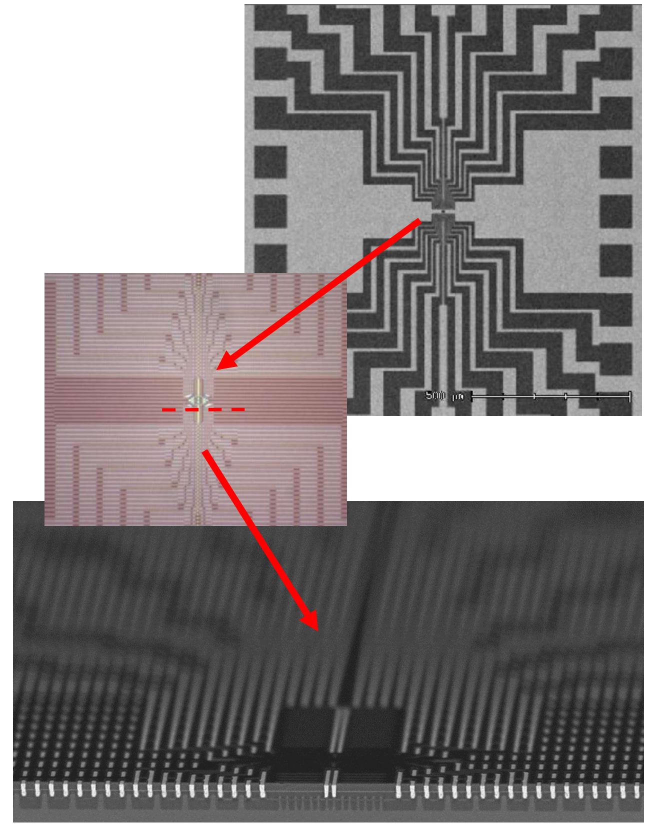


First 300mm isotopically pure silicon and world class mobility



Characterizing LAB devices





QD array devices almost ready with FAB quality Si

Developing a Quantum Computer System

Application Algorithms

Compilers/Runtimes

Control Electronics

Quantum Chip

System Metrics

Trade-offs & Constraints

Co-design for scaling

Moving to System Level Metrics

Device-level metrics

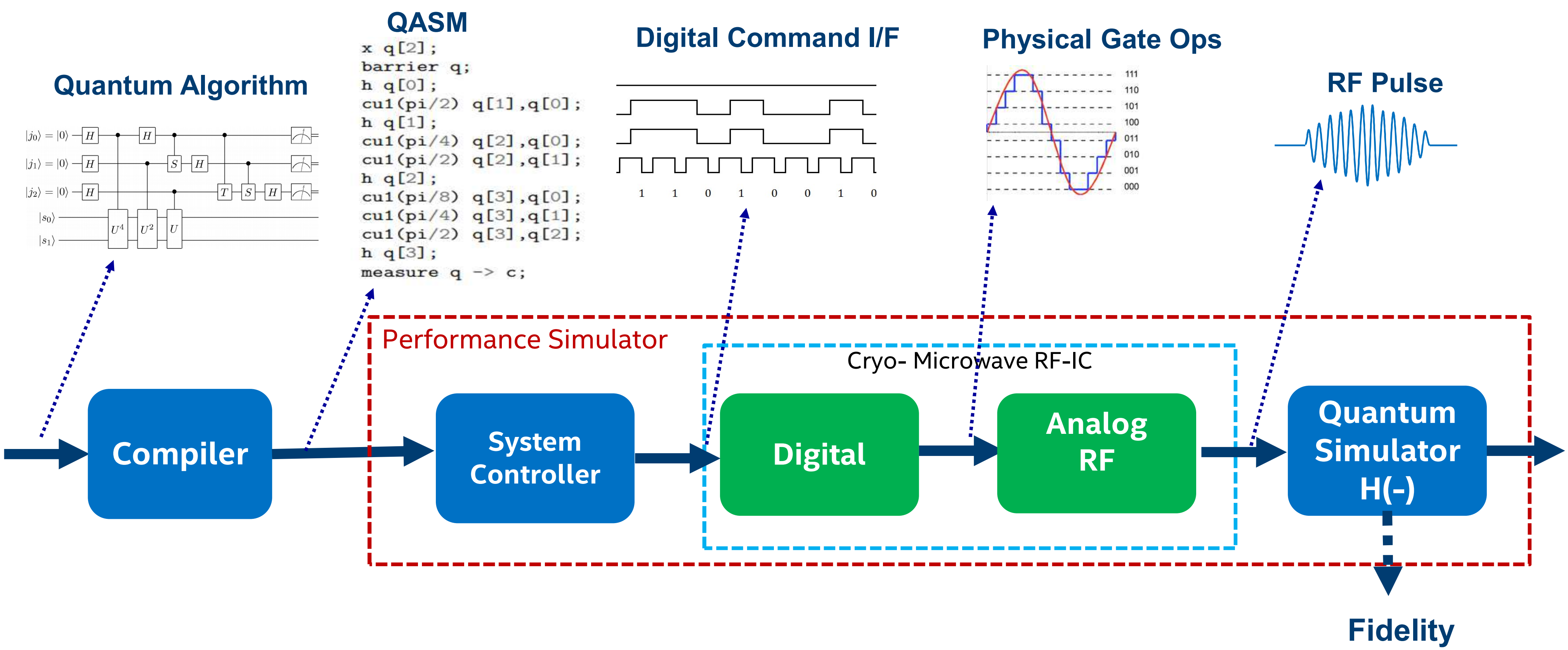
- Physical qubit count
- Decoherence time T_1, T_2

System-level metrics

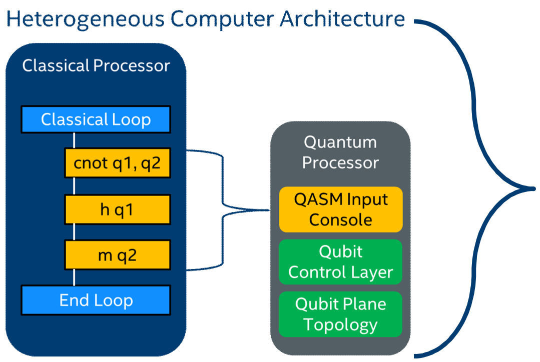
- Gate operation time
- Fidelity
- Logical qubit count
- Effective parallelization
- Utilization
- ...

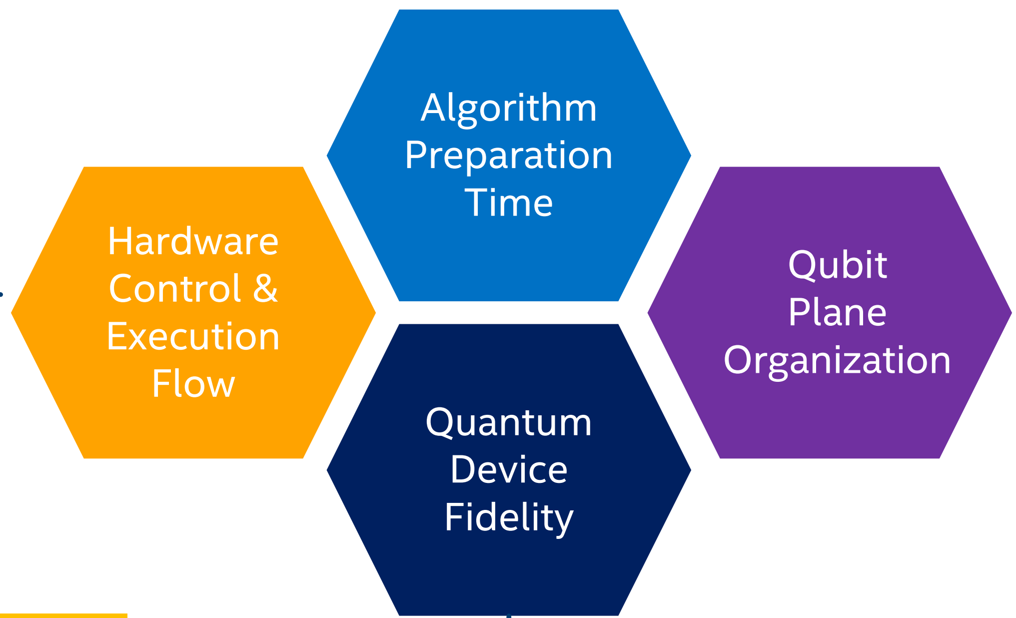
HW-SW co-design requires system metrics that impact real application performance

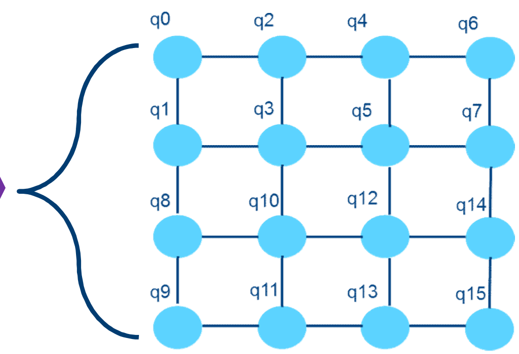
System-level performance simulation



Key Architectural Trade-Offs







Logical Op	Exec. Time (μs)	Prob. Failure
CNOT	0.01	3.07×10^{-9}
Hadamard	0.08	1.04×10^{-7}
Pauli (X,Z)	2	1.04×10^{-7}
SWP	10	2.18×10^{-4}
Teleport	150	5.06×10^{-11}
Measurement	68	1.00×10^{-6}

Realizable quantum system performance will depend heavily on the resource trade-offs we make along these attributes.

Conclusions

- The potential of quantum computing is generating tremendous excitement
- We're leveraging Intel's expertise in process and architecture to move faster
- A commercial system is ~10 Years Away

Legal Information

This presentation contains the general insights and opinions of Intel Corporation ("Intel"). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Statements in this document that refer to Intel's plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel's results and plans is included in Intel's SEC filings, including the annual report on Form 10-K.

Any forecasts of goods and services needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation. Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

intel®